DisplayPort and HDMI Compliance Test and Debug

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Agenda

- DisplayPort PHY Compliance Test
- HDMI PHY Compliance Test
- High Speed Signal Debug
DisplayPort Basics

- Data transmitted on 1, 2 or 4 differential lanes (no separate clock lines)
- Clock embedded in data lanes
- Differential AUX channel (low speed)
- First display interface to utilize packetized data transmission like Ethernet
DisplayPort Basics

- 4 lanes for data transmission
- Bit rates:
  - 1.62 Gb/s ("RBR" = reduced bit rate)
  - 2.7 Gb/s ("HBR" = high bit rate)
  - 5.4 Gb/s ("HBR2" = high bit rate 2, DisplayPort 1.2b)
  - 8.1 Gb/s ("HBR3" = high bit rate 3, DisplayPort 1.3/1.4)
- 8b/10b encoding
  - So multiply above numbers by 0.8 to get real data rate
- Clock embedded in data lanes at 1/10th bitrate (162, 270, 540 MHz, 810 MHz)
# Test Requirement

<table>
<thead>
<tr>
<th></th>
<th>DP1.2b</th>
<th>DP1.3/1.4</th>
</tr>
</thead>
<tbody>
<tr>
<td>Maximum bit rate</td>
<td>1.62Gb/s (&quot;RBR&quot; = reduced bit rate)</td>
<td>8.1Gb/s (&quot;HBR3&quot; = high bit rate 3)</td>
</tr>
<tr>
<td></td>
<td>2.7Gb/s (&quot;HBR&quot; = high bit rate)</td>
<td></td>
</tr>
<tr>
<td></td>
<td>5.4Gb/s (&quot;HBR2&quot; = high bit rate 2)</td>
<td></td>
</tr>
<tr>
<td>Number of signals to test</td>
<td>4 data lanes</td>
<td>4 data lanes</td>
</tr>
<tr>
<td>Recommend scope</td>
<td>13GHz (40GS/s)</td>
<td>16GHz (80GS/s)</td>
</tr>
<tr>
<td>bandwidth</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
Test Point Descriptions

- Five test points have been identified for physical layer measurement:
  - TP2: at the test interface on a test access fixture as close as possible to the DP mated connection to a Source device.
  - TP3: at the test interface on a test access fixture as close as possible to the DP mated connection to a Sink device.

TP3_EQ:
There are two defined cable models. One cable model is the worst cable model as defined in DP 1.2a, the other cable model is the zero length, zero loss cable. The equalizer is also defined in DP 1.2a.
VESA DisplayPort PHY Compliance Test Standard:

- 3.1 – Eye Diagram Testing
- 3.2 – Non Pre-Emphasis Level Verification Testing
- 3.3 – Pre-Emphasis Level Verification and Max Diff Pk-Pk Output Voltage
- 3.4 – Inter-Pair Skew Test (Informative)
- 3.5 – Intra-Pair Skew Test
- 3.10 – AC Common Mode Noise (Informative)
- 3.11 – Non ISI Jitter Measurements
- 3.12 – Tj, Rj and Dj Jitter Measurements
- 3.14 – Main Link Frequency
- 3.15 – SSC Modulation Frequency
- 3.16 – SSC Modulation Deviation
- 3.16 – Dual-Mode TMDS Clock Testing (If supported)
- 3.16 – Dual Mode TMDS Eye Diagram Testing (if supported)
- 8.1 – AUX Channel Eye Test
EYE Diagram & Jitter

- EYE Diagram Testing
  - RBR and HBR: TP2
  - HBR: TP3_EQ (Informative) (emulated in Analyzer SW from TP2 acquisition)
  - HBR2: TP3_EQ (emulated in Analyzer SW from TP2 acquisition)
  - HBR3: TP3_EQ (emulated in Analyzer SW from TP2 acquisition)
- The EYE Diagram test shall pass the TP3_EQ test point using both a ‘worst case’ and a ‘zero length’ cable model as described below. It is required that the source provides at least one unique setting (Voltage Swing, Pre-Emphasis Level, Post-Cursor2 Level, and Equalization) that will pass each cable model.
HBR and HBR2 Equalization:
For each of the acquisitions above, the Analyzer applies a CTLE (Continuous Time Linear Equalization) Transfer Function as defined in Figure 3-40 (for HBR) and figure 3-XX (for HBR2) of DP 1.4.

HBR3 Equalization:
For each of the acquisitions above, the Analyzer sweeps the range of CTLE (Continuous Time Linear Equalization) Transfer Functions as defined in Figure x-xx and uses the value with the optimal Eye Height (CTLE_optimal) for the compliance test result.
EYE Diagram

- Eye pattern computation

\[ \text{Diff} = \text{D}^+ - \text{D}^- \]
Main Link:
Second-order clock recovery function with a closed loop tracking bandwidth of 10MHz with a damping factor of 1.00 for HBR2
10MHz with a damping factor of 1.51 for HBR
5.4MHz with a damping factor of 1.51 for RBR
EYE Diagram

- TP2 Connection for Source Compliance Tests
### Attributes of the Signal that can be Varied

- Lane, Bitrate, Pre-emphasis, Amplitude, SSC, Test Pattern

<table>
<thead>
<tr>
<th>Bitrate</th>
<th>Pre-emph</th>
<th>Amplitude</th>
<th>SSC</th>
<th>Test Pattern</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.62</td>
<td>0</td>
<td>400mV</td>
<td>On</td>
<td>PLTPAT</td>
</tr>
<tr>
<td>2.7</td>
<td>3.5 db</td>
<td>600mV</td>
<td>Off</td>
<td>D10.2</td>
</tr>
<tr>
<td>5.4</td>
<td>6 db</td>
<td>800mV</td>
<td></td>
<td>Symbol error rate pattern</td>
</tr>
<tr>
<td>8.1</td>
<td>9.5 db</td>
<td>1200mV</td>
<td></td>
<td>CP2520</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>HBR2 Compliance</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>HBR3 Compliance</td>
</tr>
</tbody>
</table>
Current Script Requires A LOT of Manual Steps

- User will be prompted to configure their DUT settings
- They will need to do this many, many, many times.
- Result: Compliance Testing is MANUAL and not AUTOMATIC and is not competitive
The QPHY-DisplayPort software provides an automated test environment for running all of the normative real-time oscilloscope tests for sources in accordance with Version 1.2b of the Video Electronics Standards Association (VESA) DisplayPort PHY Compliance Test Specification, as well as tests for HBR3 signals at 8.1 Gbps.

- Support for RBR, HBR, HBR2, and HBR3 bit rates (1.62 Gb/s, 2.7 Gb/s, 5.4 Gb/s, and 8.1 Gb/s)
- Support for testing of 1, 2 or 4 lanes
- 100% automated testing using Unigraf DPR-100 with AUX Control capability
DP Test Fixture

- Wilder Technologies
  - [http://www.wilder-tech.com/dp-kits.htm](http://www.wilder-tech.com/dp-kits.htm)

- Key Electrical
  - 1.35Gb/s, 2.7Gb/s, 5.4Gb/s, and 8.1Gb/s data rates supported
  - Insertion loss $< -3\text{dB}$ @ 6.5GHz / Return loss $< -20\text{dB}$ @ 4.25GHz
  - Differential Impedance 100+/-5 ohms / Single Ended Impedance 50+/-2.5 ohms
AUX Controller and switch matrix

- "Automation" - Automatic configuration of DUT settings using AUX controller - Unigraf DPR-100 Reference Sink, Commands DUT via AUX lines to go into appropriate modes, No manual user-configurations required!
  - Aux controller
    - https://www.unigraf.fi/products/dp-test-hardware/dpr-100
    - DPR-100 is operating as a DP AUX Controller to automate the DP PHY testing with a compliant PHY Test Equipment. With the AUX Controller firmware DPR-100 is compatible with TeledyneLeCroy oscilloscopes
  - Switch Matrix
    - Mini-circuits Switch Matrix support for 4-lane testing
      - No connect/disconnect of cabling!
The QualiPHY software application automates the oscilloscope setup, test and report generation.

Bit Rate / OutputLevel / Pre-emphasis / Pattern / SSC are configured by Aux controller.
Connection Diagram with Switch and AUX Controller

- QualiPHY displays connection diagrams to ensure tests run properly
## Summary Table

<table>
<thead>
<tr>
<th>Pass#</th>
<th>Test Description</th>
<th>Lane</th>
<th>Speed</th>
<th>SSC</th>
<th>Nom Output Level</th>
<th>Nom Preemp</th>
<th>Current Value</th>
<th>Test Criteria</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>HBR3 TPS4 Non-ISI Jitter (UI)</td>
<td>Lane0</td>
<td>8.1Gb/s</td>
<td>Enabled</td>
<td>400mV</td>
<td>[Unknown Variable]</td>
<td>161.0 mUI</td>
<td>x &lt; 560.0 mUI</td>
</tr>
<tr>
<td>1</td>
<td>HBR3 TPS4 TP3_EQ Eye Diagram Testing, Worst Case Cable</td>
<td>Lane0</td>
<td>8.1Gb/s</td>
<td>Enabled</td>
<td>400mV</td>
<td>3.5dB</td>
<td>0 hits</td>
<td>x = 0 hits</td>
</tr>
<tr>
<td>1</td>
<td>HBR3 TPS4 Worst Case Cable Total Jitter (UI)</td>
<td>Lane0</td>
<td>8.1Gb/s</td>
<td>Enabled</td>
<td>400mV</td>
<td>3.5dB</td>
<td>577.2 mUI</td>
<td>x &lt; 650.0 mUI</td>
</tr>
<tr>
<td>1</td>
<td>HBR3 TPS4 Worst Case Cable Random Jitter (UI)</td>
<td>Lane0</td>
<td>8.1Gb/s</td>
<td>Enabled</td>
<td>400mV</td>
<td>3.5dB</td>
<td>13.5 mUI</td>
<td>x &lt; 160.0 mUI</td>
</tr>
<tr>
<td>1</td>
<td>HBR3 TPS4 TP3_EQ Eye Diagram Testing, Zero Length</td>
<td>Lane0</td>
<td>8.1Gb/s</td>
<td>Enabled</td>
<td>400mV</td>
<td>3.5dB</td>
<td>0 hits</td>
<td>x = 0 hits</td>
</tr>
<tr>
<td>1</td>
<td>HBR3 TPS4 Zero Length Total Jitter (UI)</td>
<td>Lane0</td>
<td>8.1Gb/s</td>
<td>Enabled</td>
<td>400mV</td>
<td>3.5dB</td>
<td>507.9 mUI</td>
<td>x &lt; 650.0 mUI</td>
</tr>
<tr>
<td>1</td>
<td>HBR3 TPS4 Zero Length Random Jitter (UI)</td>
<td>Lane0</td>
<td>8.1Gb/s</td>
<td>Enabled</td>
<td>400mV</td>
<td>3.5dB</td>
<td>16.3 mUI</td>
<td>x &lt; 160.0 mUI</td>
</tr>
</tbody>
</table>
DisplayPort Over Type-C

- Example for interface that supports USB and DisplayPort Alternate Mode
- Similar switch needed at the Device end
- Switch can be integrated along with the USB and DisplayPort functions
USB Type-C DP ALT Mode Test Fixture

- Wilder Tech
  http://www.wilder-tech.com/dpc-kits.htm
Embedded DisplayPort

- eDP is a variant of DisplayPort that is used for internal interfaces
  - For example, from a laptop’s graphics card to its integrated flat-panel display

- eDP compliance tests are a subset of DisplayPort tests

- The current Compliance Test Guideline (CTG) version for eDP is 1.4a
  - This is easy to confuse with “regular” DisplayPort, which is at version 1.3
    - they are numbered independently
Test Fixture

- Fixtures are available from Wilder Technologies

- eDP connectors come in 40-pin or 50-pin flavors – your customer should know which one they need
Agenda

- DisplayPort PHY Compliance Test
- HDMI PHY Compliance Test
- High Speed Signal Debug
HDMI Structure

Transmitter

TP1

TMDS (AV Link)

TP2

Sink (Display)

Ck Frequency = Data Rate/N

HDMI2.0:

Data Rates: 3.4 Gbs to 6Gbs

N=40

xN PLL

Data TX

SDA

SCL

DDC GND

Reserved

HPD

CEC

Ck

E-DDC (i2c)

Ethernet/Audio Return Channel

EDID

HDCP

SCDC

HEC/ARC

+V

CEC Controller
## HDMI Basics

<table>
<thead>
<tr>
<th></th>
<th>HDMI 1.4b</th>
<th>HDMI 2.0</th>
</tr>
</thead>
<tbody>
<tr>
<td>Maximum bit rate</td>
<td>3.4 Gb/s</td>
<td>6.0 Gb/s</td>
</tr>
<tr>
<td>Number of signals to test</td>
<td>3 data + 1 clock</td>
<td>3 data + 1 clock</td>
</tr>
<tr>
<td>Required scope bandwidth</td>
<td>8 GHz</td>
<td>13 GHz</td>
</tr>
<tr>
<td>Required input adapter</td>
<td>TF-HDMI-3.3V</td>
<td>TF-HDMI-3.3V</td>
</tr>
</tbody>
</table>

### Diagram

![HDMI Diagram](image-url)
HDMI 源端一致性测试

- HDMI 1.3/1.4 Source 端测试
  - 低电平输出电压(7-2)
  - 上升时间/下降时间(7-4)
  - 信号对间时间偏移(7-6)
  - 信号对内时间偏移(7-7)
  - 时钟占空比(7-8)
  - 时钟抖动(7-9)
  - 眼图(7-10)

- HDMI 2.0 Source 端测试
  - 低电平输出电压和摆幅(HF1-1)
  - 上升时间/下降时间(HF1-2)
  - 信号对间时间偏移(HF1-3)
  - 信号对内时间偏移(HF1-4)
  - 差分电压测试（HF1-5）
  - 时钟占空比(HF1-6)
  - 时钟抖动(HF1-7)
  - 眼图(HF1-8)
测试点的变化
HDMI 2.0 Eye diagram Test Requirement

<table>
<thead>
<tr>
<th>TMDS Bit Rate (Gbps)</th>
<th>H (T_{bit})</th>
<th>V (mV)</th>
</tr>
</thead>
<tbody>
<tr>
<td>3.71</td>
<td>0.6</td>
<td>335</td>
</tr>
<tr>
<td>4.46</td>
<td>0.56</td>
<td>295</td>
</tr>
<tr>
<td>5.94</td>
<td>0.4</td>
<td>150</td>
</tr>
</tbody>
</table>

Others

See [HDMI 2.0: Table 6-5]
TP1 Connection for Source Compliance Tests
- Apply the Worst Cable Emulator to measure TMDS differential signals at TP2 eye
新的测试要求

- HDMI2.0测试所需要的示波器带宽：不低于13GHz
- HDMI2.0增加了TP2EQ测试点，要求在信号经过最差的线缆之后，并且经过均衡处理之后，再去测量
- 测试设备有多种分辨率需要测试：
  - HDMI1.4需要测试27M (or 25M), 74.25M,148.5M,222.75MHz
  - HDMI2.0 需要测试370M,594M
For compliance testing, the HDMI source must be controlled to output the correct signals for each test.

For those who cannot, they will need to use an Extended Display Identification Data (EDID) controller, which talks to the source over the HDMI link and tells it what to output.

- Granite River Labs HDMI-CONT for EDID control
- HDMI-EDID-EMS (Source (Host) Emulator)
  - [http://www.wilder-tech.com/hdmi-a-20-kits.htm](http://www.wilder-tech.com/hdmi-a-20-kits.htm)
Switch matrix

- Mini-circuits RC-8SPDT-A18
  - Since HDMI testing requires both single-ended and differential measurements on 4 differential signals, we need to measure 8 signals total
  - QPHY-HDMI2 has functionality built in to control a switch matrix for this purpose
- Using the switch matrix also requires a separate HDMI termination module, the Wilder Technologies HDMI-TPA-T
  - http://www.wilder-tech.com/hdmi-a-20-kits.htm
TF-HDMI-3.3V 50 ohms Pull-up Terminator

- The TF-HDMI-3.3V adapter provides the necessary 3.3 V pull-up termination for HDMI testing.
- The TF-HDMI-3.3V provides both a signal path through to the oscilloscope with a 3.3 V pull-up termination as well as an input that is directly terminated to 3.3 V. This is required for terminating the data lines that are not currently under test.
- The TF-HDMI-3.3V-QUADPAK provides four adapters and 8 SMA-SMA cables to allow for the testing of all HDMI signals (Clock, D0, D1 and D2).
QualiPHY = The TOTAL PC Solution

- QualiPHY = QPHY = An electrical (PHY) Compliance serial data standard package **SOLUTION**

The QualiPHY software application automates the oscilloscope setup, test and report generation.

QualiPHY displays connection diagrams to ensure tests run properly.
## Summary Table

<table>
<thead>
<tr>
<th>Pass</th>
<th>Run #</th>
<th>Test</th>
<th>Measurement</th>
<th>Current Value</th>
<th>Test Criteria</th>
</tr>
</thead>
<tbody>
<tr>
<td>✔</td>
<td>1</td>
<td>HF1-1 Char Rate Check, VL, Vswing, D0</td>
<td></td>
<td>371.0 Mcps</td>
<td>340.0 Mcps &lt;= x &lt;= 600.0 Mcps</td>
</tr>
<tr>
<td>✔</td>
<td>1</td>
<td>HF1-1 VL Measurement, D0+</td>
<td></td>
<td>2.780 V</td>
<td>2.300 V &lt; x &lt; 2.900 V</td>
</tr>
<tr>
<td>✔</td>
<td>1</td>
<td>HF1-1 Vswing Measurement, D0+</td>
<td></td>
<td>460 mV</td>
<td>400 mV &lt; x &lt; 600 mV</td>
</tr>
<tr>
<td>✔</td>
<td>1</td>
<td>HF1-1 VL Measurement, D0-</td>
<td></td>
<td>2.769 V</td>
<td>2.300 V &lt; x &lt; 2.900 V</td>
</tr>
<tr>
<td>✔</td>
<td>1</td>
<td>HF1-1 Vswing Measurement, D0-</td>
<td></td>
<td>470 mV</td>
<td>400 mV &lt; x &lt; 600 mV</td>
</tr>
<tr>
<td>✔</td>
<td>1</td>
<td>HF1-1 VL Measurement, CLK+</td>
<td></td>
<td>2.790 V</td>
<td>2.300 V &lt; x &lt; 3.100 V</td>
</tr>
<tr>
<td>✔</td>
<td>1</td>
<td>HF1-1 Vswing Measurement, CLK+</td>
<td></td>
<td>429 mV</td>
<td>200 mV &lt; x &lt; 600 mV</td>
</tr>
<tr>
<td>✔</td>
<td>1</td>
<td>HF1-1 VL Measurement, CLK-</td>
<td></td>
<td>2.789 V</td>
<td>2.300 V &lt; x &lt; 3.100 V</td>
</tr>
<tr>
<td>✔</td>
<td>1</td>
<td>HF1-1 Vswing Measurement, CLK-</td>
<td></td>
<td>437 mV</td>
<td>200 mV &lt; x &lt; 600 mV</td>
</tr>
<tr>
<td>✔</td>
<td>1</td>
<td>HF1-5 Differential Voltage Vmin check, D0</td>
<td></td>
<td>-561 mV</td>
<td>x &gt;= -780 mV</td>
</tr>
</tbody>
</table>
Agenda

- DisplayPort PHY Compliance Test
- HDMI PHY Compliance Test
- High Speed Signal Debug
### Compliance Test-Mask Test Issue

<table>
<thead>
<tr>
<th>Test Case</th>
<th>Category</th>
<th>Value</th>
<th>Result</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.3.3.1</td>
<td>Rj (rms) CP0 SigTest</td>
<td>1.555 ps</td>
<td>x &lt;= 3.270 ps</td>
</tr>
<tr>
<td>1.3.3.2</td>
<td>Di DD CP0 SigTest</td>
<td>56.36 ps</td>
<td>x &lt;= 86.00 ps</td>
</tr>
<tr>
<td>1.3.3.3</td>
<td>Min Time Between Crossovers (after channel) SigTest</td>
<td>125.987 ps</td>
<td>Informational Only</td>
</tr>
<tr>
<td>1.3.3.4</td>
<td>Avg UI SigTest</td>
<td>200.3924 ps</td>
<td>Informational Only</td>
</tr>
<tr>
<td>1.3.3.5</td>
<td>Max PP Jitter SigTest</td>
<td>82.036 ps</td>
<td>Informational Only</td>
</tr>
<tr>
<td>1.3.5</td>
<td>Non Trans Violations SigTest</td>
<td>0 hits</td>
<td>x = 0 hits</td>
</tr>
<tr>
<td>1.3.5</td>
<td>Trans Violations SigTest</td>
<td>33.043 kHz</td>
<td>x = 0 hits</td>
</tr>
<tr>
<td>1.3.5</td>
<td>Max Non Trans Voltage SigTest</td>
<td>186.3 mV</td>
<td>Informational Only</td>
</tr>
</tbody>
</table>

![Diagram](image-url)
Debugging issues with Jitter, Noise and Crosstalk

- To find the root cause of failures/problems:
  - You need to dig deeper than Eye diagrams, Tj, Rj, Dj, …
  - These are aggregate results

- Understand jitter/noise sources using “multi-domain analysis”
  - Time domain
  - Frequency domain
  - Shape of jitter distribution
  - Data dependent effects

Your oscilloscope has additional views of jitter in addition to Tj/Rj/Dj
Today’s Scenario to Debug

- Expect eye diagram to look like this:

- But instead see this:
Serial Data Jitter Analysis & Debug

- Requires Deep, Accurate Insight Into Jitter Breakdown

![Diagram of Jitter Breakdown]

- **Tj** (Total Jitter)
  - **Rj** (Random Jitter)
  - **Dj** (Deterministic Jitter)
    - **BUj** (Bounded Uncorrelated Jitter)
      - **Pj** (Periodic Jitter)
      - **OBUj** (Other BUj)
    - **DDj** (Data Dependent Jitter)
      - **DCD** (Duty Cycle Distortion)
      - **ISI** (InterSymbol Interference)
InterSymbol Interference (ISI) Basics

- Signature: Jitter on an edge function of bit history
  - TIE Track repeats for a repeating pattern (e.g., PRBS7)

- Bounded. And depends on data

- Causes:
  - Reflections change the shape of an edge
  - Limited channel bandwidth
  - Know the single bit response of your channel
Signal Frequency of NRZ data and bit pattern

Data rate = 5Gbps

2.5GHz

1.25GHz

833MHz

1bit -> 1U:200ps
Considering low pass filter as simple as CR circuit.

Signal edge is slowed down by time constant of the CR circuit.
Duty Cycle Distortion (DCD) Basics

- Signature: two states in TIE Track and histogram
- Measures difference in bit width for 0 and 1 bits
- Bounded.
- Caused by:
  - Variation in crossing level and/or shift in signal’s offset
Periodic Jitter Basics

- Signature: pks in spectrum, bowl-shape histogram
- Bounded.
- Called Pj; pure sinusoidal would be SJ
- Caused by:
  - Coupling in of other periodic signals in system
  - Power supply switching frequency
Understanding Random Jitter

- **Signature:** Gaussian tails on jitter histogram
- **Unbounded…. Gaussian**

**Causes:**
- Thermal noise, shot noise, flicker noise
- Random variations in otherwise uniform structures
- Deterministic jitter contributors create an overall distribution with Gaussian tails.
Most Complete Jitter, Eye and Analysis Toolkit

- Most complete jitter, eye diagram and analysis tools
- Up to four simultaneous eyes
- Fastest eye diagram creation
- Up to 4-lane measurement and analysis
- Unique Reference Lane and LaneScape Comparison Mode
- Vertical noise measurements
- Crosstalk analysis
Most Complete Jitter, Eye and Analysis Toolkit
Use Case: Single lane in circuit → Multiple Analysis Scenarios

Scenario 1: Use measurement
Scenario 2: Use Emphasis
Scenario 3: Use CTLE
Scenario 4: Use DFE
Single lane in the circuit → Multiple Analysis Scenarios
Apply Equalization and De-embed / Emulate Fixtures & Channels

- SDAIII-CompleteLinQ seamlessly integrates transmitter emphasis and receiver equalization features
- Use EyeDoctorII or the new VirtualProbe package
Channel Emulation

- Measured at end of reference channel and cables at TP1
Apply Equalization with Eye Doctor II

- SDAIII-CompleteLinQ seamlessly integrates transmitter emphasis and receiver CTLE, FFE and DFE equalizers.
1. For very fast data rates (>5 Gb/s), the transmitter signal typically has very good signal integrity. However, after propagating through the backplane, this signal will become severely degraded.

2. At the far end of the channel, the eye is closed. The signal at the receiver pins (which can be probed) is not the signal of interest. The equalized signal inside of the receiver chip (which cannot be probed) is the signal of interest.

3. The equalized signal within the receiver chip cannot be probed. How can this signal be validated to ensure low jitter, a clean eye pattern, and good signal integrity?
EyeDoctor™ II and VirtualProbe Signal Integrity Tools

VirtualProbe shows you the signal where the probe is not located:

1. Fixture
2. Backplane
3. Connector
4. Trace

Virtually probe the signal at the transmitter with the fixture present, and then de-embed its effects form the measurement.

View the signal between structures to understand losses, ISI and crosstalk caused by backplanes, interconnects and connectors.

See what the eye looks like at the receiver—even if it is not in reach of a differential probe.

Use EyeDoctor to open the eye by modeling CTLE, FFE and DFE equalizers used by your receiver.
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