DisplayPort PHY Validation

TELEDYNE LECROY
Everywhere you look™

立肯科技
LeColn Technology
## DisplayPort Basics

<table>
<thead>
<tr>
<th></th>
<th>DP1.2b</th>
<th>DP1.3/1.4</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Maximum bit rate</strong></td>
<td>1.62Gb/s (“RBR” = reduced bit rate)</td>
<td>8.1Gb/s (“HBR3” = high bit rate 3)</td>
</tr>
<tr>
<td></td>
<td>2.7Gb/s (“HBR” = high bit rate)</td>
<td></td>
</tr>
<tr>
<td></td>
<td>5.4Gb/s (“HBR2” = high bit rate 2)</td>
<td></td>
</tr>
<tr>
<td><strong>Number of signals to test</strong></td>
<td>4 data lanes</td>
<td>4 data lanes</td>
</tr>
<tr>
<td><strong>Required scope bandwidth</strong></td>
<td>13GHz</td>
<td>16GHz</td>
</tr>
</tbody>
</table>
Five test points have been identified for physical layer measurement:

- **TP2**: at the test interface on a test access fixture as close as possible to the DP mated connection to a Source device.
- **TP3**: at the test interface on a test access fixture as close as possible to the DP mated connection to a Sink device.

**TP3_EQ:**
There are two defined cable models. One cable model is the worst cable model as defined in DP 1.2a, the other cable model is the zero length, zero loss cable. The equalizer is also defined in DP 1.2a.
DP PHY Compliance Test Standard

- VESA DisplayPort PHY Compliance Test Standard:
  - 3.1 – Eye Diagram Testing
  - 3.2 – Non Pre-Emphasis Level Verification Testing
  - 3.3 – Pre-Emphasis Level Verification and Max Diff Pk-Pk Output Voltage
  - 3.4 – Inter-Pair Skew Test
  - 3.5 – Intra-Pair Skew Test
  - 3.10 – AC Common Mode Noise
  - 3.11 – Non ISI Jitter Measurements
  - 3.12 – Tj, Rj and Dj Jitter Measurements
  - 3.14 – Main Link Frequency
  - 3.15 – SSC Modulation Frequency
  - 3.16 – SSC Modulation Deviation
  - 3.16 – Dual-Mode TMDS Clock Testing
  - 3.16 – Dual Mode TMDS Eye Diagram Testing
  - 8.1 – AUX Channel Eye Test
EYE Diagram & Jitter

- **EYE Diagram Testing**
  - RBR and HBR: TP2
  - HBR: TP3_EQ (emulated in Analyzer SW from TP2 acquisition)
  - HBR2: TP3_EQ (emulated in Analyzer SW from TP2 acquisition)
  - HBR3: TP3_EQ (emulated in Analyzer SW from TP2 acquisition)

- The EYE Diagram test shall pass the TP3_EQ test point using both a ‘worst case’ and a ‘zero length’ cable model as described below. It is required that the source provides at least one unique setting (Voltage Swing, Pre-Emphasis Level, Post-Cursor2 Level, and Equalization) that will pass each cable model.
**EYE Diagram**

- **Eye pattern computation**

![Diagram showing eye pattern computation with labels for D+, D-, and Diff = D+ - D-]
Main Link:
Second-order clock recovery function with a closed loop tracking bandwidth of 10MHz with a damping factor of 1.00 for HBR2
10MHz with a damping factor of 1.51 for HBR
5.4MHz with a damping factor of 1.51 for RBR

UI = one bit time
TP2 Connection for Source Compliance Tests

TP2
TP3 Worst Cable
TP3 Worst Cable + EQ

TX
D+
D+
Transmitter De-emphasis

- Loss and Channel BW - Worst Cable Model
Transmitter De-emphasis

- Loss and Channel BW - Worst Cable Model

Diagram showing the process of de-emphasis involving transmitter, cable, and receiver with TP2 and TP3 components.
Transmitter De-emphasis

- De-emphasis and Worst Cable model

0dB
3.5dB
6dB
9.5dB
Jitter Measurement

- Total jitter ($T_j$) is a measure of the maximum peak-to-peak jitter at a specified bit error rate (BER), for example $T_j = n*R_j + D_j$ (BER=10^-9)
Jitter Measurement

- **Deterministic Jitter**
  - Obtain DJ PDF via deconvolution and associated pk-pk (directly from jitter PDF, or derivative of BER CDF)
Jitter Measurement

- Tj, Rj and Dj & Non ISI Jitter Measurements
### Attributes of the Signal that can be Varied

- Lane, Bitrate, Pre-emphasis, Amplitude, SSC, Test Pattern

<table>
<thead>
<tr>
<th>Bitrate</th>
<th>Pre-emph</th>
<th>Amplitude</th>
<th>SSC</th>
<th>Test Pattern</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.62</td>
<td>0</td>
<td>400mV</td>
<td>On</td>
<td>PLTPAT</td>
</tr>
<tr>
<td>2.7</td>
<td>3.5 db</td>
<td>600mV</td>
<td>Off</td>
<td>D10.2</td>
</tr>
<tr>
<td>5.4</td>
<td>6 db</td>
<td>800mV</td>
<td></td>
<td>Symbol error rate pattern</td>
</tr>
<tr>
<td>8.1</td>
<td>9.5 db</td>
<td>1200mV</td>
<td></td>
<td>CP2520</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>HBR2 Compliance</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>HBR3 Compliance</td>
</tr>
</tbody>
</table>
Automation PHY Validation

- The QPHY-DisplayPort software provides an automated test environment for running all of the normative real-time oscilloscope tests for sources in accordance with Version 1.2b of the Video Electronics Standards Association (VESA) DisplayPort PHY Compliance Test Specification, as well as tests for HBR3 signals at 8.1 Gbps.
- Support for RBR, HBR, HBR2, and HBR3 bit rates (1.62 Gb/s, 2.7 Gb/s, 5.4 Gb/s, and 8.1 Gb/s)
- Support for testing of 1, 2 or 4 lanes
- 100% automated testing using Unigraf DPR-100 with AUX Control capability
DP Test Fixture

- Wilder Technologies
  - [http://www.wilder-tech.com/dp-kits.htm](http://www.wilder-tech.com/dp-kits.htm)

- Key Electrical
  - 1.35Gb/s, 2.7Gb/s, 5.4Gb/s, and 8.1Gb/s data rates supported
  - Insertion loss < -3dB @ 6.5GHz / Return loss < -20dB @ 4.25GHz
  - Differential Impedance 100+/−5 ohms / Single Ended Impedance 50+/−2.5 ohms
AUX Controller and switch matrix

- “Automation” - Automatic configuration of DUT settings using AUX controller - Unigraf DPR-100 Reference Sink, Commands DUT via AUX lines to go into appropriate modes, No manual user-configurations required!
  - Aux controller
    - [https://www.unigraf.fi/products/dp-test-hardware/dpr-100](https://www.unigraf.fi/products/dp-test-hardware/dpr-100)
    - DPR-100 is operating as a DP AUX Controller to automate the DP PHY testing with a compliant PHY Test Equipment. With the AUX Controller firmware DPR-100 is compatible with TeledyneLeCroy oscilloscopes
  - Switch Matrix
    - Mini-circuits Switch Matrix support for 4-lane testing
    - No connect/disconnect of cabling!
The QualiPHY software application automates the oscilloscope setup, test and report generation. Bit Rate / OutputLevel / Pre-emphasis / Pattern / SSC are configured by Aux controller.
QualiPHY displays connection diagrams to ensure tests run properly.
# Summary Table

<table>
<thead>
<tr>
<th>Pass#</th>
<th>Test</th>
<th>Measurement</th>
<th>Lane</th>
<th>Speed</th>
<th>SSC</th>
<th>Nom Output Level</th>
<th>Nom Preemp</th>
<th>Current Value</th>
<th>Test Criteria</th>
<th>Nom Preemp</th>
<th>Current Value</th>
<th>Test Criteria</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>(3.11)</td>
<td>HBR3 TPS4 Non-ISI Jitter (UI)</td>
<td>Lane0</td>
<td>8.1G/s</td>
<td>Enabled</td>
<td>400mV</td>
<td>[Unknown Variable]</td>
<td>161.0 mUI</td>
<td>x &lt; 560.0 mUI</td>
<td>x = 0 hits</td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>(3.1)</td>
<td>HBR3 TPS4 TP3_EQ Eye Diagram Testing, Worst Case Cable</td>
<td>Lane0</td>
<td>8.1G/s</td>
<td>Enabled</td>
<td>400mV</td>
<td>3.5dB</td>
<td>0 hits</td>
<td>x = 0 hits</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>(3.12.1)</td>
<td>HBR3 TPS4 Worst Case Cable Total Jitter (UI)</td>
<td>Lane0</td>
<td>8.1G/s</td>
<td>Enabled</td>
<td>400mV</td>
<td>3.5dB</td>
<td>577.2 mUI</td>
<td>x &lt; 650.0 mUI</td>
<td>x &lt; 160.0 mUI</td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>(3.12.1)</td>
<td>HBR3 TPS4 Worst Case Cable Random Jitter (UI)</td>
<td>Lane0</td>
<td>8.1G/s</td>
<td>Enabled</td>
<td>400mV</td>
<td>3.5dB</td>
<td>13.5 mUI</td>
<td>x &lt; 160.0 mUI</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>(3.1)</td>
<td>HBR3 TPS4 TP3_EQ Eye Diagram Testing, Zero Length</td>
<td>Lane0</td>
<td>8.1G/s</td>
<td>Enabled</td>
<td>400mV</td>
<td>3.5dB</td>
<td>0 hits</td>
<td>x = 0 hits</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>(3.12.1)</td>
<td>HBR3 TPS4 Zero Length Total Jitter (UI)</td>
<td>Lane0</td>
<td>8.1G/s</td>
<td>Enabled</td>
<td>400mV</td>
<td>3.5dB</td>
<td>507.9 mUI</td>
<td>x &lt; 650.0 mUI</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>(3.12.1)</td>
<td>HBR3 TPS4 Zero Length Random Jitter (UI)</td>
<td>Lane0</td>
<td>8.1G/s</td>
<td>Enabled</td>
<td>400mV</td>
<td>3.5dB</td>
<td>16.3 mUI</td>
<td>x &lt; 160.0 mUI</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
USB Type-C DP ALT Mode Test Fixture

- Luxshare-ICT
  - Type-C connector
  - DisplayPort ALT mode
  - Type-C to DP dongle
### HDMI Basics

<table>
<thead>
<tr>
<th>Feature</th>
<th>HDMI 1.4b</th>
<th>HDMI 2.0</th>
</tr>
</thead>
<tbody>
<tr>
<td>Maximum bit rate</td>
<td>3.4 Gb/s</td>
<td>6.0 Gb/s</td>
</tr>
<tr>
<td>Number of signals to test</td>
<td>3 data + 1 clock</td>
<td>3 data + 1 clock</td>
</tr>
<tr>
<td>Required scope bandwidth</td>
<td>8 GHz</td>
<td>13 GHz</td>
</tr>
<tr>
<td>Required input adapter</td>
<td>TF-HDMI-3.3V</td>
<td>TF-HDMI-3.3V</td>
</tr>
</tbody>
</table>

![HDMI Diagram](image)
Test Point Descriptions

- The signal test points for a TMDS link are shown below.
  - TP1 is used for testing of HDMI Sources and Transmitter components.
  - TP2 is used for testing of HDMI Sinks and Receiver components.
  - TP1 and TP2 together are also used for testing of cables.
HDMI1.4 TMDS Electrical Compliance

- 7-2: VL
- 7-4: TRise, TFall
- 7-5: Over/Undershoot (Not Mandatory)
- 7-6: Inter-Pair Skew
- 7-7: Intra-Pair Skew
- 7-8: Clock Duty Cycle
- 7-9: Clock Jitter
- 7-10: Data Eye Diagram
HDMI2.0 TMDS Electrical Compliance

- HF1-1: VL and Vswing
- HF1-2: Trise Tfall
- HF1-3: Inter-pair Skew
- HF1-4: Intra-pair Skew
- HF1-5: Differential Voltage
- HF1-6: Clock Duty Cycle
- HF1-7: Clock Jitter
- HF1-8: Data Eye Diagram
TP1 Connection for Source Compliance Tests

- Apply the Worst Cable Emulator to measure TMDS differential signals at TP2 eye.
Wilder Technologies


Key Electrical:

- 4.95Gb/s and 10.2Gb/s data rates supported
- Insertion loss < -3dB @ 9.6GHz / Return loss < -20dB @ 3.3GHz
- Differential Impedance 100+/-5ohms / Single Ended Impedance 50+/-2.5 ohms
EDID controller

- For compliance testing, the HDMI source must be controlled to output the correct signals for each test.
- For those who cannot, they will need to use an Extended Display Identification Data (EDID) controller, which talks to the source over the HDMI link and tells it what to output.
  - Granite River Labs HDMI-CONT for EDID control
  - HDMI-EDID-EMS (Source (Host) Emulator)
    - [http://www.wilder-tech.com/hdmi-a-20-kits.htm](http://www.wilder-tech.com/hdmi-a-20-kits.htm)
Switch matrix

- Mini-circuits RC-8SPDT-A18
  - Since HDMI testing requires both single-ended and differential measurements on 4 differential signals, we need to measure 8 signals total
  - QPHY-HDMI2 has functionality built in to control a switch matrix for this purpose
- Using the switch matrix also requires a separate HDMI termination module, the Wilder Technologies HDMI-TPA-T
  - [http://www.wilder-tech.com/hdmi-a-20-kits.htm](http://www.wilder-tech.com/hdmi-a-20-kits.htm)
The TF-HDMI-3.3V adapter provides the necessary 3.3 V pull-up termination for HDMI testing.

The TF-HDMI-3.3V provides both a signal path through to the oscilloscope with a 3.3 V pull-up termination as well as an input that is directly terminated to 3.3 V. This is required for terminating the data lines that are not currently under test.

The TF-HDMI-3.3V-QUADPAK provides four adapters and 8 SMA-SMA cables to allow for the testing of all HDMI signals (Clock, D0, D1 and D2).
QualiPHY = The TOTAL PC Solution

- QualiPHY = QPHY = An electrical (PHY) Compliance serial data standard package SOLUTION

The QualiPHY software application automates the oscilloscope setup, test and report generation.

QualiPHY displays connection diagrams to ensure tests run properly.
# Summary Table

<table>
<thead>
<tr>
<th>Pass</th>
<th>Run #</th>
<th>Test</th>
<th>Measurement</th>
<th>Current Value</th>
<th>Test Criteria</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>HF1-1</td>
<td>Char Rate Check, VL, Vswing, D0</td>
<td></td>
<td>371.0 Mcps</td>
<td>340.0 Mcps &lt;= x &lt;= 600.0 Mcps</td>
</tr>
<tr>
<td>1</td>
<td>HF1-1</td>
<td>VL Measurement, D0+</td>
<td></td>
<td>2.780 V</td>
<td>2.300 V &lt; x &lt; 2.900 V</td>
</tr>
<tr>
<td>1</td>
<td>HF1-1</td>
<td>Vswing Measurement, D0+</td>
<td></td>
<td>460 mV</td>
<td>400 mV &lt; x &lt; 600 mV</td>
</tr>
<tr>
<td>1</td>
<td>HF1-1</td>
<td>VL Measurement, D0-</td>
<td></td>
<td>2.769 V</td>
<td>2.300 V &lt; x &lt; 2.900 V</td>
</tr>
<tr>
<td>1</td>
<td>HF1-1</td>
<td>Vswing Measurement, D0-</td>
<td></td>
<td>470 mV</td>
<td>400 mV &lt; x &lt; 600 mV</td>
</tr>
<tr>
<td>1</td>
<td>HF1-1</td>
<td>VL Measurement, CLK+</td>
<td></td>
<td>2.790 V</td>
<td>2.300 V &lt; x &lt; 3.100 V</td>
</tr>
<tr>
<td>1</td>
<td>HF1-1</td>
<td>Vswing Measurement, CLK+</td>
<td></td>
<td>429 mV</td>
<td>200 mV &lt; x &lt; 600 mV</td>
</tr>
<tr>
<td>1</td>
<td>HF1-1</td>
<td>VL Measurement, CLK-</td>
<td></td>
<td>2.789 V</td>
<td>2.300 V &lt; x &lt; 3.100 V</td>
</tr>
<tr>
<td>1</td>
<td>HF1-1</td>
<td>Vswing Measurement, CLK-</td>
<td></td>
<td>437 mV</td>
<td>200 mV &lt; x &lt; 600 mV</td>
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<tr>
<td>1</td>
<td>HF1-5</td>
<td>Differential Voltage Vmin check, D0</td>
<td></td>
<td>-561 mV</td>
<td>x &gt;= -780 mV</td>
</tr>
</tbody>
</table>

Report (Sample of HDMI2.0)
High Speed Serial Bus Debug
Section 1 - Probing

LeColn, Service and Support Division
WaveLink® Hi-BW Differential Probing System (13GHz – 25GHz)

- Example of D2505-A-PS
1. Connecting the Amplifier Module to the Platform/Cable Assembly

2. Connecting a solder-in interconnect lead to an amplifier module

NOTE:
• The entire SI tip should be positioned with the resistor side upright facing (away from the PCB plane).
• Keep a 45 degree angle between the SI tip ends and the PCB plane.
Caution: This configuration has non-standard leads added to probes which are not matched, and add inductance.

A probe with flat geometry and rubberized flex circuit lead can be easily secured in place.

- Adhesive base mount
- Tips soldered to chip pins
- Probing discrete components
Caution: This configuration has non-standard leads added to probes which are not matched, and add inductance.

When damping resistors are removed for connection to the interposer, the leads should be replaced with 3mm 34 gauge wire.
Caution: Using square pin or other adapters which reduce rated bandwidth can reduce measurement accuracy.

Square pin connectors are typically rated at 3GHz BW.

Solder-in tip rated at 13 GHz bandwidth.
Teledyne LeCroy’s Dxx05-PT positioner tip browser can be easily hand-held with the attachable wand or positioned in place with one of many standard or optional accessory mechanical positioners.
Serial Data Jitter Analysis & Debug

- Requires Deep, Accurate Insight Into Jitter Breakdown

Compliance Testing

Debug & Analysis

Tj (Total Jitter)

Rj (Random Jitter)

Dj (Deterministic Jitter)

BUj (Bounded Uncorrelated Jitter)

DDj (Data Dependent Jitter)

Pj (Periodic Jitter)

OBUj (Other BUj)

DCD (Duty Cycle Distortion)

ISI (InterSymbol Interference)
Continuous Bit Eye Pattern Rendering

- Real Time Eye (consecutive UI)

A block of continuous serial data is acquired. Bits are separated using software clock recovery. Overlapped bits form the eye pattern.
Total Jitter

- Total jitter is a measure of the maximum peak-to-peak jitter at a specified bit error rate (BER).
- The specified BER is another way of expressing a confidence interval or observation time.
- Total jitter is determined by integrating the probability density function (PDF) separately from the left and right sides to determine the cumulative probability density (CDF).
- The width of this curve at the specified BER (or confidence interval) gives the total jitter.
Histogram Growth

Source: JitterTime Consulting

Gaussian Statistics Reference Table

<table>
<thead>
<tr>
<th>BER</th>
<th>DTD = 50% (Most Data)</th>
<th>DTD = 100% (Clocks)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1E-1</td>
<td>2.563</td>
<td>3.290</td>
</tr>
<tr>
<td>1E-2</td>
<td>4.653</td>
<td>5.152</td>
</tr>
<tr>
<td>1E-3</td>
<td>6.180</td>
<td>6.581</td>
</tr>
<tr>
<td>1E-4</td>
<td>7.438</td>
<td>7.781</td>
</tr>
<tr>
<td>1E-5</td>
<td>8.530</td>
<td>8.834</td>
</tr>
<tr>
<td>1E-6</td>
<td>9.507</td>
<td>9.783</td>
</tr>
<tr>
<td>1E-7</td>
<td>10.399</td>
<td>10.653</td>
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<tr>
<td>1E-8</td>
<td>11.224</td>
<td>11.461</td>
</tr>
<tr>
<td>1E-9</td>
<td>11.996</td>
<td>12.219</td>
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<td>1E-10</td>
<td>12.723</td>
<td>12.934</td>
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<td>1E-11</td>
<td>13.412</td>
<td>13.613</td>
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<td>1E-12</td>
<td>14.069</td>
<td>14.261</td>
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<td>1E-13</td>
<td>14.698</td>
<td>14.882</td>
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<td>1E-14</td>
<td>15.301</td>
<td>15.479</td>
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<tr>
<td>1E-15</td>
<td>15.883</td>
<td>16.054</td>
</tr>
<tr>
<td>1E-16</td>
<td>16.444</td>
<td>16.610</td>
</tr>
</tbody>
</table>
Jitter Components

- Separation of random and deterministic jitter
  - \( T_j = N \times R_j + D_j \)
  - \( N \) = sigma value for selected BER
  - \( D_j \) = p-p deterministic jitter
  - Approximate “heuristic” formula
- Measure \( T_j \) at several BER values and solve for \( R_j \) and \( D_j \)
Jitter Analysis Component of Dj : ISI (Inter-Symbol Interference)

- Edge shift made by former data pattern is called as “ISI”
- It is typical in cases of insufficient bandwidth.
Jitter Analysis Component of Dj : DDj (Data Dependent jitter)
SDA3 = Sigtest + Advance Analysis Tools

- Transition Eye / Non-Transition Eye / Jitter are as same as Sigtest
Apply Equalization and De-embed / Emulate Fixtures & Channels

- SDAIII-CompleteLinQ seamlessly integrates transmitter emphasis and receiver equalization features
- Use EyeDoctorII or the new VirtualProbe package
Channel Emulation

- Measured at end of reference channel and cables at TP1

Import S-parameter (S4P)
Apply Equalization with Eye Doctor II

- SDAIII-CompleteLinQ seamlessly integrates transmitter emphasis and receiver CTLE, FFE and DFE equalizers
1. For very fast data rates (>5 Gb/s), the transmitter signal typically has very good signal integrity. However, after propagating through the backplane, this signal will become severely degraded.

2. At the far end of the channel, the eye is closed. The signal at the receiver pins (which can be probed) is not the signal of interest. The equalized signal inside of the receiver chip (which cannot be probed) is the signal of interest.

3. The equalized signal within the receiver chip cannot be probed. How can this signal be validated to ensure low jitter, a clean eye pattern, and good signal integrity?
EyeDoctor™ II and VirtualProbe Signal Integrity Tools

VirtualProbe shows you the signal where the probe is not located:

1. Fixture
2. Backplane
3. Connector
4. Trace

Virtually probe the signal at the transmitter with the fixture present, and then de-embed its effects from the measurement.

View the signal between structures to understand losses, ISI and crosstalk caused by backplanes, interconnects and connectors.

See what the eye looks like at the receiver—even if it is not in reach of a differential probe.

Use EyeDoctor to open the eye by modeling CTLE, FFE and DFE equalizers used by your receiver.
High Speed Serial Bus Debug

Section 3 – WaveScan
(Advanced Search and Analysis)

LeColn, Service and Support Division
Auto Parameters, but not smart

- Scope captures lots of cycles, Why Rise Time(20%-80%) is only 29ps?
Smart Parameter

- Statistic ON = Full Cycles/Screen measurement

First screen = 24,832
Second screen = 24,801
Third screen = 24,768
Fourth screen = 24,866

......You get every Rise Times via Smart Parameter!

Statistic num = 24,832
Statistic num = 24,832+24,801
Statistic num = 24,832+24,801+24,768
Statistic num = 24,832+24,801+24,768+24,866
How can I view and analysis waveforms >40ps Rise Time (20% - 80%)?
Wavescan = Smart Waveform scan capability

- Scans for an event in many acquisitions over a long period of time. It supports 6 search modes, apply a search condition and begin scanning is very simple.
Finds Problems That Triggers Won't Find

- A Teledyne LeCroy X-Stream oscilloscope will quickly scan millions of events, looking for unusual occurrences, and do it much faster and more efficiently than other oscilloscopes can.
High Speed Serial Bus Debug

Section 4 – LabNotebook
(Flashback tool)

LeColn, Service and Support Division
Our users can efficiently create complete and detailed waveform reports directly in the oscilloscope. An all-in-one solution for annotating and sharing information, LabNotebook simplifies results recording and report generation by eliminating the multi-step processes that often involve several pieces of equipment.

- Save Waveforms = Keep Datas
- Save Table = Keep Parameters values
- Save Setup = Keep scope setups
- Print Screen = Keep the pictures

Labnotebook
- = Save waveforms + Table + Setup + Print Screen
- And + Report Generator
Flashback is one of the most powerful features in LeCroy’s LabNotebook documentation tool. Not only does LabNotebook save a report of a user selected test, it also can store the acquired waveforms and oscilloscope setup. If you find yourself in the position of having not taken a specific measurement during the test, with Flashback you can recall the data and make additional measurements.
LabNotebook enables the users to focus on results:

- Save all display waveforms
- Save the relevant DSO setup with saved waveforms
- Add freehand notes with a stylus
- Convert the complete report to PDF, HTML, RTF
- Print or e-mail reports
I forgot to measure Fall Time(20%-80%) before Power Off

- Fortunately, You created a Labnotebook entry before Power Off